Mixed-signal Neural Decoder

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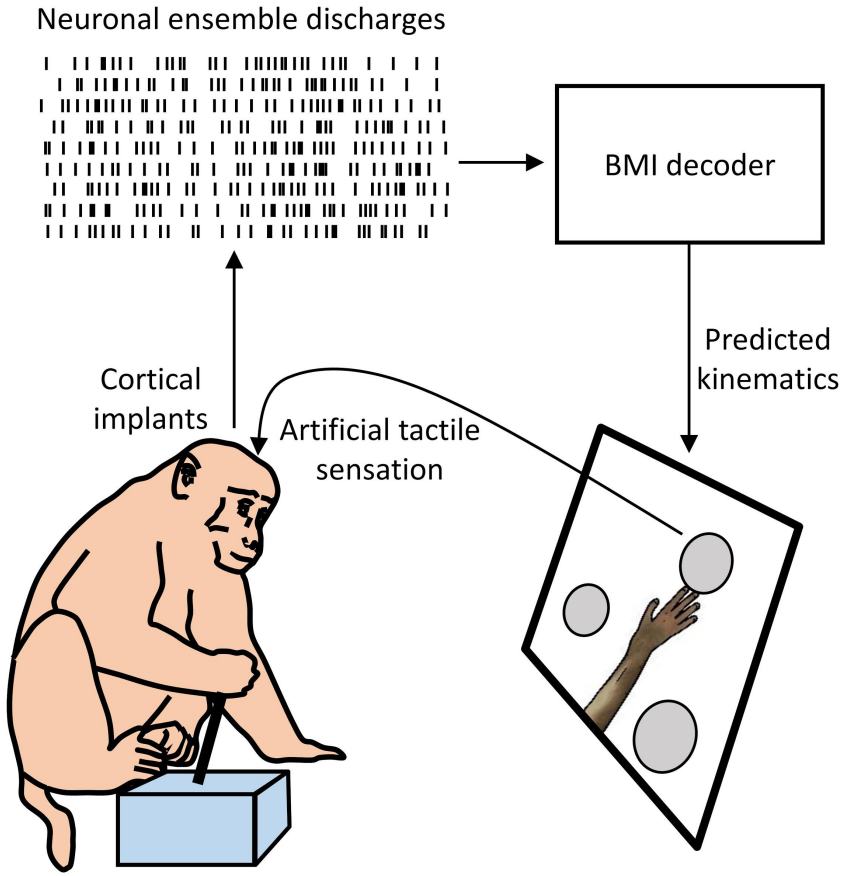
Motivation

- Neural Decoding: reconstruction of sensory stimuli from recorded neural information.
- Applications: brain-machine interface, prosthetics, understanding of neurological disorders (epilepsy)



What we plan to achieve (I)

- A low power neural decoding ASIC suitable for implantation
- Why low power?
  - Low power elongates battery life
  - Too much power damages brain tissue (0.4 mW/mm^2 upper limit)
  - Tissue damage is correlated with temperature, so we should strive for lower power

What we plan to achieve (II)

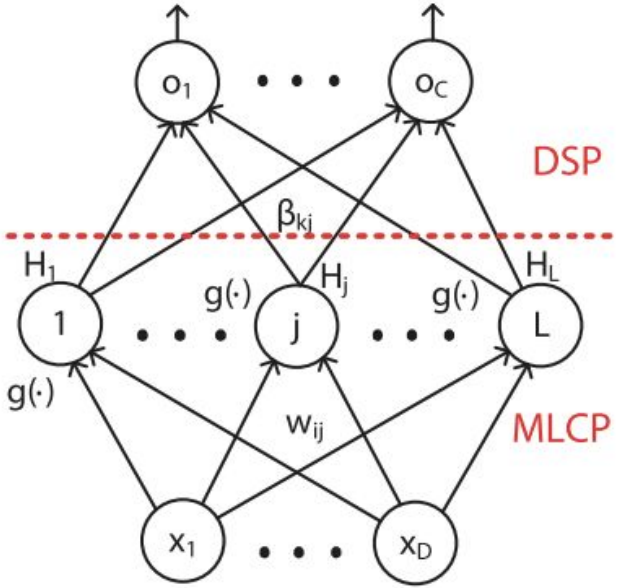
- Why ASIC?
  - FPGAs tend to consume more power

Author	Implementation	Power
P. Wolf (2008)	Spike Sorting on FPGA	0.96 mW/channel
Moo Sung Chae et al (2009)	Spike feature extraction with DSP	46 µW/channel
Yi Chen et al (2016)	Mixed signal neural decoding	0.003 µW/channel

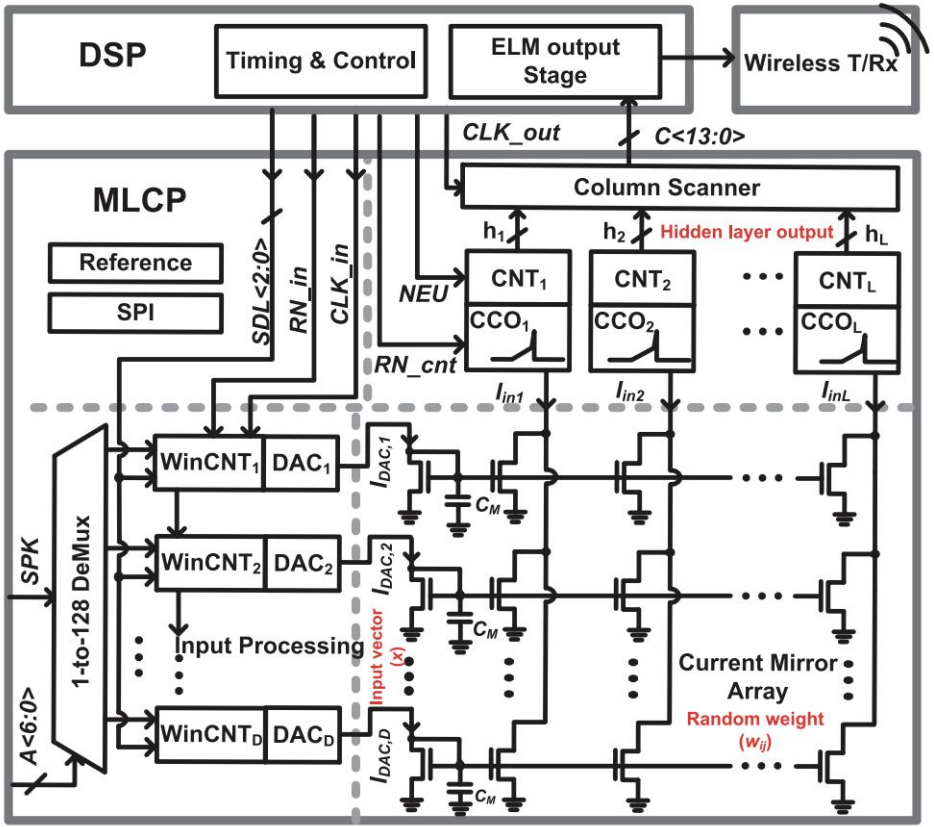
  - FPGAs are not implantable, thus systems where most of the computation are done on FPGA require wireless data transfer

Extreme Learning Machine

- The algorithm:
  - Single hidden layer feedforward neural network
  - Hidden layer implemented on a machine learning coprocessor (MLPC)
  - Input layer weights generated randomly from mismatch of current mirrors
  - Output layer implemented on DSP processor



Chip level implementation



Design Process

- Data acquisition: Spike train data available from online sources
  - Data set recorded from anterior lateral motor cortex of mice
  - Data set contains 32 channels
- Software: Implement ELM in software first so later we can verify our hardware works
  - MATLAB
- Verilog-AMS level implementation: Translate the algorithm into hardware
  - Write good verilog

Design Process cont.

- Circuit level design: Replace verilog components with transistor level schematics
- Verification: Collect hidden layer output from chip and simulate output layer on software to verify trained data
- Layout: Once schematic has been simulated and verified, implement custom layout to minimize area

Specifications

Process technology	45nm GPDK	Target area	5 mm^2
Target power/area	0.4mW/mm^2	VDD	1.2V analog, 1V digital
Spike train channel number	32	Clock frequency	50 Hz
Maximum spike train frequency	640 Hz	Sampling window	100 ms
Window counter resolution	6 bits	DAC resolution	6 bits
Hidden layer node number	128		